THAT WHICH IS CLAIMED IS:

1. A method of controlling interrupts generated by a peripheral, comprising:

storing, in an interrupt pending register, active bits corresponding to interrupt flags generated by said peripheral;

sending to an interrupt control circuit coupled to said peripheral an interrupt signal obtained by ORing said interrupt flags;

upon receiving said interrupt signal said interrupt control circuit, identifying and serving the interrupt;

characterized in that it further comprises generating a respective bit string identifying an active bit corresponding to the interrupt that must be served; and

serving the interrupt corresponding to said bit string.

2. The method of claim 1, wherein said bit string identifies the position of the first active bit in said interrupt pending register of the peripheral that requested the interrupt.

3. The method of claim 1, comprising the step of generating a second bit string identifying the position of the last active bit in said interrupt pending register of the peripheral that requested the interrupt.

4. The method of claim 1, comprising the step of generating a third bit string identifying the number of active bits in said interrupt pending

register of the peripheral that requested the interrupt.

5. The method of claim 1, comprising the steps of:

once the peripheral that generated the relative interrupt flag has been identified, copying the content of the interrupt pending register of the peripheral in an auxiliary register; and

generating said bit string in function of the content of said auxiliary register.

6. An auxiliary interrupt control circuit, connectable to an interrupt control circuit, to a microprocessor and to at least a peripheral having an interrupt pending register, said control circuit receiving an interrupt signal corresponding to the logic OR of interrupt flags stored in said interrupt pending register, said auxiliary circuit comprising:

an encoding circuit coupled to said interrupt pending register of the peripheral, sending to said microprocessor a bit string encoding the position of an active bit stored in said interrupt pending register corresponding to a certain interrupt to be served.

7. The auxiliary circuit of claim 6, further comprising:

an auxiliary register, the size of which coincides to that of the interrupt pending register of the connected peripheral, for storing the content of said interrupt pending register;

said encoding circuit being coupled to said auxiliary register and said bit string encoding the position of an active bit stored in said auxiliary

register.

8. The auxiliary circuit of claim 6, comprising a first register in which to store said bit string encoding the position of the first active bit in said interrupt pending register.

9. The auxiliary circuit of claim 6, comprising a second register in which to store a second bit string encoding the position of a last active bit in said interrupt pending register.

10. The auxiliary circuit of claim 6, comprising a third register in which to store a third bit string generated by said encoding circuit (ENCODER) encoding the number of active bits in said interrupt pending register.

11. The auxiliary circuit of claim 6, further comprising an interrupt priority mask circuit, said first bit string encoding the position of an active bit corresponding to a pending interrupt of highest priority.

12. The auxiliary circuit of claim 11, further comprising a writable memory storing the priority values provided by said interrupt control circuit stored, said interrupt priority mask circuit depending on which peripheral generated an interrupt being configured in function of respective priority values stored in said writable memory.

13. A peripheral connectable to a microprocessor and to an interrupt control circuit,

associated to an interrupt pending register, said interrupt control circuit receiving an interrupt signal corresponding to the logic OR of interrupt flags generated by the peripheral and stored in said interrupt pending register, characterized in that it comprises an auxiliary control circuit as defined in claim 6.

14. A microprocessor system, comprising an interrupt control circuit, a plurality of peripherals each being associated to a respective interrupt pending register, said control circuit receiving respective interrupt signals corresponding to the logic OR of interrupt flags stored in the respective interrupt pending register, a microprocessor coupled to said control circuit and to said peripherals, characterized in that it comprises:

an auxiliary control circuit as defined in claim 6 coupled to said peripherals and sending to said microprocessor a bit string encoding the position of an active bit stored in the interrupt pending register of the peripheral that generated the interrupt.